REMARKS

Claims 4, 5, 6, 8, 9, and 13-24 are pending in this application. Claims 1-3, 7, 10-12, were previously cancelled and claims 21-24 are added herein. Claim 17 has been amended herein. In view of these amendments and remarks, Applicant respectfully requests reconsideration of the claims.

Claim 17 was rejected under 35 U.S.C. 112, second paragraph as being indefinite. However, claim 17 has been corrected and is no longer indefinite.

Claims 8-9 and 15 were rejected under 35 U.S.C. 102(b) as being anticipated by Morishima. Applicant disagrees. More specifically, claims 8-9 and 15 were also rejected over Morishima under 35 U.S.C. 102(b) in the previous Office Action. In response to that rejection arguments were filed on November 24, 2005 to distinguish these claims from Morishima. However, contrary to Applicant's arguments, the Examiner is of the opinion that the Morishima reference "shows a bipolar pulse (input pulse) with a positive part and a negative part (high or low) of the same duration...". However, the Applicant's specification and drawings clearly indicate that there is a reference potential or ground and that the potential of the positive part of the input pulse is greater than the reference potential or ground, and the potential of the negative part of the input pulse is less than the reference potential or ground. Thus, the term bipolar as used in the specification has a clear meaning. Namely, the signal has two polarities (i.e., a positive part, such as for example +VDD, and a negative part, such as for example –VDD). This, of course, also fits the definition from the Webster's Unabridged Dictionary, "Having two poles." On the other hand, FIG. 3A of Morishima shows an input signal V1 that changes between 0 volts and VDD, with a midpoint of VDD/2.

In addition, it is submitted that in accordance with the wording of claim 8 as well as in accordance with the wording of claim 15, a "difference signal" is to be generated on the basis of the input signal and the delayed signal. Morishima clearly does not disclose such an approach, despite disclosing the provision of a delay circuit 7 and a differential circuit 20. As can be seen from FIG. 1, the differential amplifier circuit receives three input signals V1, V9, and V10. However, it is clear from the description given with regard to FIG. 3 of Morishima, that no difference signal is generated at the output of the amplifier. The output signal is termed V6 and the waveform thereof is shown as FIG. 3F. The input signal is signal V1 also shown in FIG. 3A and the delayed signal is signal V10 shown in FIG. 3C. Comparing the two signal waveforms shown in FIGs. 3A and 3C clearly shows that the output signal V6 is not the difference between the signal waveforms in FIGs. 3A and 3C.

Therefore, Morishima certainly does not disclose a device for generating a difference signal on the basis of an input signal and a delayed signal as required by claims 8 and 9. In addition, Morishima does not disclose the possibility of decoding a bit by means of the different signal as required in claim 15. Further, Morishima does not disclose a termination load as required in claims 8 and 0. The Examiner is of the opinion that Morishima describes in column 10, lines 20-24 the provision of such a termination load. It is respectfully submitted that this is not correct as this portion of Morishima only specifies that the delay circuit 7 may have more inverters connected in series to another of resistors, capacitors, and the like to increase the delay time. Thus, the elements mentioned at the give portion in Morishima are not termination loads. Rather, these elements can only be considered as part of the delay line.

Therefore, it is submitted that claims 8-9 and 15 do patentably define over the Morisihima reference.

All of the claims 4-6, 8-9, and 13-28 were rejected under 35 U.S.C. 102(b) as being anticipated by Goto. Again, Applicant disagrees. Goto concerns a timing adjustment circuit 8, as is shown in FIG. 1. This circuit comprises a fine delay means 81, a coarse delay means 82, and a selection means 9'. As stated at column 6, lines 48-52 of the specification, the selection means is for selecting delay signals from one of the coarse delay elements. Thus, the basic purpose of Goto is to provide a signal having a combined delay on the basis of the input signal, which is subject to the fine delay and on the basis of a selected signal, which is subjected to a coarse delay. Thus, the basic operation of the selection means 9' is to select the signals that are to be combined with each other.

The Examiner is also of the opinion that block 9' of FIG. 1 forms a differential amplifier in the sense of the present application. This is simply incorrect, nothing with regard to a differential amplifier in block 9' can be derived from any portion of the specification of the Goto reference. Further, block 9' does not generate a difference signal on the basis of an input signal and a delayed signal, and the differential amplifier does not include an edge detector for detecting an edge of the partially delayed signal. With respect to the detection of a rising edge, the Examiner's reference to column 8, lines 5-9, which clearly specifies that output signals s4 to s7 are provided upon detecting a rising edge of the output signal p0 of the fine delay means. Therefore, Goto clearly does not disclose the detection of an edge of a partially delayed signal, i.e., a signal subjected to one or more of the coarse delay elements. Goto includes nothing with regard to the comparator for determining as to whether the different signal is greater than a predetermined threshold. Further, nothing in Goto teaches or suggests that a threshold signal could be applied to the block 9'. Therefore, it is submitted that the Examiner's conclusion that

Goto anticipates the subject matter of pending claim 4 simply is not correct. Goto neither teaches nor suggests the inventive device as defined in claim 4.

With respect to claim 8, Goto, as mentioned above, clearly does not disclose a device for generating a difference signal on the basis of the input signal and the delayed signal. Therefore, Goto cannot anticipate the subject matter of claim 8.

For the same reasons discussed with regard to claim 4 and 15, Goto cannot anticipate the subject matter of claim 13 or the subject matter of claim 15.

Claim 16, of course, also includes the feature of the differential amplifier and, in addition, the last element of claim 16 refers to defining the selection of the respective input signals depending on the duration of the respective parts of the bipolar pulse. Goto does not even mention, much less teach such a feature.

Likewise, claims 17 and 18 both include the feature of the differential amplifier, and in addition claim 18 also includes an element requiring an edge detector and a comparator. Therefore, for the same reasons discussed above, Goto does not anticipate the subject matter of claims 17 and 18.

Therefore, it is submitted that the subject matter as defined in the present claims is clearly structurally different from the disclosure of Goto and these claims are clearly allowable over Goto.

Claims 16 and 17 were further rejected under 35 U.S.C. 102(b) as being anticipated by Zhang, *et al.* Applicant also respectfully disagrees that Zhang even makes obvious, much less teaches the invention described in claim 16 and 17. Zhang discloses a delay generator as shown in FIG. 1, which outputs a plurality of delayed signals 110, 120. One of these signals is selected by multiplexer 170 (see column 3, lines 14 to 17). However, Zhang teaches a differential

amplifier receiving two input signals for generating a difference signal as defined in claims 16 and 17. Further, nothing is derivable from Zhang with regard to selecting one of a plurality of first input signals and selecting one of a plurality of special input signals depending on the duration of the positive part and the negative part of the bipolar input pulse.

Therefore, since Zhang does not disclose the above-mentioned features, Zhang cannot anticipate the subject matter either of claim 16 or 17. Thus, the Examiner's conclusion that the subject matter of claims 16 and 17 is structurally identical to the disclosure of reference 3 is incorrect.

In view of the above, Applicant respectfully submits that the application is in condition for allowance and requests that the Examiner pass the case to issuance. If the Examiner should have any questions, Applicant requests that the Examiner contact Applicant's attorney at 972-732-1001 so that such issues may be resolved as expeditiously as possible. No fee is believed due in connection with this filing. However, in the event that there are any fees due, please charge the same, or credit any overpayment, to Deposit Account No. 50-1065.

Respectfully submitted,

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Date

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